

DT15 Rec'd PCT/PTO 15 JUL 2004

XA-10097
PATENT APPLICATION #2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Michitaro KANAMITSU et al.

Intl. Appln. No.: PCT/JP02/01846

Intl. Filing Date: 28 February 2002

For: NONVOLATILE SEMICONDUCTOR STORAGE UNIT

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INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Attn: Mail Stop PCT, DO/EO/US

Sir:

Pursuant to 37 C.F.R. § 1.56, and without any
assertion as to materiality or prior art effect, the
documents listed on the attached Form PTO-1449 are hereby
cited.

Documents AH-AJ on the attached List were cited in the
International Search Report (copy attached).

Documents AO-AQ (copies herewith) are cited in the

specification, on page 2, and their relevance is indicated therein.

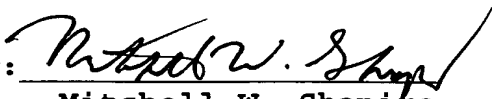
Respectfully submitted,

MWS:jab

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July 15, 2004

By:


Mitchell W. Shapiro
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| FORM PTO-1449 | | Atty. Docket No. XA-10097 | Appln. No. 38/501391 |
| LIST OF DOCUMENTS CITED BY APPLICANT | | Applicant Michitaro KANAMITSU et al. | |
| | | Filing Date Herewith | Group |

U.S. PATENT DOCUMENTS

| Examiner Initial | | Document Number | Date | Name | Class | Sub-class | Filing Date |
|------------------|----|-----------------|------|------|-------|-----------|-------------|
| | AA | | | | | | |
| | AB | | | | | | |
| | AC | | | | | | |
| | AD | | | | | | |
| | AE | | | | | | |
| | AF | | | | | | |
| | AG | | | | | | |

FOREIGN PATENT DOCUMENTS

| Examiner Initial | | Document Number | Date | Country | Class | Sub-class | Translation |
|------------------|----|-----------------|----------|---------|-------|-----------|-------------|
| | AH | 11-250681 | 9/17/99 | Japan | | | No |
| | AI | 7-307098 | 11/21/95 | Japan | | | No |
| | AJ | 10-188576 | 7/21/98 | Japan | | | No |
| | AK | | | | | | |
| | AL | | | | | | |
| | AM | | | | | | |
| | AN | | | | | | |

OTHER (including author, title, date, pertinent pages, etc.)

| | |
|----|--|
| AO | K. Imamiya et al., "MP6.6 A 130mm ² 256 Mb NAND Flash with Shallow Trench Isolation Technology", <u>1999 IEEE International Solid-State Circuits Conference</u> . |
| AP | K. Suh et al., "TA7.5: A 3.3V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme", <u>1995 IEEE International Solid-State Circuits Conference</u> , pp. 128-129. |
| AQ | K. Imamiya et al., "TA7.6: A 35 ns-Cycle-Time 3.3V-Only 32 Mb NAND Flash EEPROM", <u>1995 IEEE International Solid-State Circuits Conference</u> , pp. 130-131. |

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|----------|-----------------|
| Examiner | Date Considered |
|----------|-----------------|

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.